**Design and Characterization of On-Chip Antennas for System-on-Chip Applications**

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In the last few years, the increased level of integration provided by silicon technologies and emerging applications at millimeter wave frequencies has helped to achieve true System-on-Chip solutions bringing the antennas on the chip. This is because antenna sizes at these frequencies become small enough for practical on-chip realization. At the same time, there are a number of challenges to overcome, for instance co-design with circuits and integration in small form factors, low efficiency issues due to silicon substrate losses, layout restrictions, on-chip characterization to name a few. This half-day short course aims to discuss the above challenges in detail and propose some solutions as well. It includes a comprehensive overview of state-of-the-art in the field and discusses the upcoming trends in on-chip antennas from an applications perspective where they are being used in Terahertz, implantable, MEMS and Energy Harvesting applications. A number of design examples such as 5 GHz transceivers with on-chip antennas (130nm CMOS), 12 GHz power amplifier with integrated antenna (GaN), 60 GHz PLL with on-chip antenna (65nm CMOS), 77 GHz vertical on-chip antenna (MEMS) and 94 GHz superstrate loaded on-chip antenna (Low and High Res Si) will be presented. Our recently accepted paper titled ‘*On-Chip Antennas: The Last Barrier*, in IEEE Microwave Magazine (to appear in Jan 2013) also reflects the significance of on-chip antennas for antennas community.

**Learning Objective**: Participants will comprehend the design and characterization challenges associated with designing on-chip antennas. They will also learn about some RF and mm wave on-chip antenna designs in various processes and for different applications.

**Presentation and Materials:** Power point slides will be provided to the participants.